WHAT IS CLAIMED IS:

1. A method for forming one or more FinFET devices, comprising:

forming a source region and a drain region in an oxide layer, the oxide layer being disposed on a substrate;

etching the oxide layer between the source region and the drain region to form a plurality of oxide walls, the areas between the plurality of oxide walls defining a plurality of respective channels for a first device;

depositing a connector material over the plurality of oxide walls and channels for the first device;

forming a gate mask for the first device;

removing the connector material from the channels;

depositing channel material in the channels for the first device;

forming a gate dielectric for first device over the channels;

depositing a gate material over the gate dielectric for the first device; and

patterning and etching the gate material to form at least one gate electrode for the first device.

2. The method of claim 1 wherein the forming a source region and a drain region includes:

forming the source region and a drain region to a depth ranging from about 1000 Å to about 2000 Å into the oxide layer.

3. The method of claim 1 wherein the forming a source region and a drain region includes:

etching the oxide layer to form a source area and a drain area,

filling the source area and the drain area with a first material.

4. The method of claim 1 wherein the etching the oxide layer between the source region and the drain region terminates at a depth of the source region and the drain region.

5. The method of claim 1 wherein a depth of the channels ranges from about 1000 Å to about 2000 Å into the top surface of the oxide layer.

6. The method of claim 1 further comprising:

filling, prior to depositing a gate mask, openings in the channels with a sacrificial material, and

wherein the removing the connector material includes:

removing the sacrificial material and the connector material from the channels.

7. The method of claim 1 further comprising:

repeating, for a second device, the forming a source region and a drain region in the oxide layer; etching the oxide layer between the source region and the drain region; depositing a connector material over the plurality of oxide walls and channels; forming a gate mask; removing the connector material; depositing channel material; forming a gate dielectric over the channel material; depositing a gate material over the gate dielectric; and patterning and etching the gate material to form at least one gate electrode.

8. The method of claim 1 wherein the source region and the drain region are used by the first device and a second device.

9. The method of claim 8 further comprising:

repeating, for the second device, the etching the oxide layer between the source region and the drain region to form a plurality of oxide walls and channels; depositing a connector material over the plurality of oxide walls and channels; forming a gate mask; removing the connector material; depositing channel material; forming a gate dielectric over the channel material; depositing a gate material over the gate dielectric; and patterning and etching the gate material to form at least one gate electrode.

10. A method of manufacturing a semiconductor device that includes a substrate and a first layer formed on the substrate, comprising:

etching the first layer to form a source area and a drain area;

filling the source and drain areas with a first material to form source and drain regions;

forming a plurality of channels in the first layer between the source region and the drain region;

depositing a connector material over the first layer between the source region and the drain region;

forming a gate mask over the first layer between the source region and the drain region;

removing the connector material in the plurality of channels;

depositing a channel material in the plurality of channels;

forming a gate dielectric over the channel material;

depositing a gate material over the gate dielectric; and

patterning and etching the gate material to form at least one gate electrode.

11. The method of claim 10 wherein a depth of the source area and the drain area ranges from about 1000 Å to about 2000 Å into an upper surface of the first layer.

12. The method of claim 10 wherein a depth of each of the plurality of channels ranges from about 1000 Å to about 2000 Å into an upper surface of the first layer.

13. The method of claim 10 wherein the first layer comprises one of an oxide and a nitride.

14. The method of claim 10 wherein a number of the plurality of channels is based on a width of the source region and the drain region.

15. The method of claim 10 further comprising:

repeating the etching the first layer to form a source area and a drain area; filling the source and drain areas with a first material to form source and drain regions; forming a plurality of channels in the first layer between the source region and the drain region; depositing a connector material over the first layer between the source region and the drain region; forming a gate mask over the first layer between the source region and the drain region; removing the connector material in the plurality of channels; depositing a channel material in the plurality of channels; forming a gate dielectric over the channel material; depositing a gate material over the gate dielectric; and patterning and etching the gate material to form at least one gate electrode for a second semiconductor device.

16. The method of claim 10 wherein the source region and the drain region are shared by the semiconductor device and a second semiconductor device.

17. The method of claim 16 further comprising:

repeating the forming a plurality of channels in the first layer between the source region and the drain region; depositing a connector material over the first layer between the source region and the drain region; forming a gate mask over the first layer between the source region and the drain region; removing the connector material in the plurality of channels; depositing a channel material in the plurality of channels; forming a gate dielectric over the channel material; depositing a gate material over the gate dielectric; and patterning and etching the gate material to form at least one gate electrode for a second semiconductor device.

18. A method for forming two devices on a substrate having a first layer formed thereon, the first layer comprising one of an oxide and a nitride, the method comprising:

forming a source region and a drain region in the first layer for a first device and a second device;

forming a plurality of channels for the first device in the first layer between the source region and the drain region;

depositing connector material for the first device over the first layer between the source region and the drain region;

forming a gate mask for the first device over the first layer between the source region and the drain region;

removing the connector material from the plurality of channels;

depositing channel material for the first device in the plurality of channels;

forming a gate dielectric over the channel material for the first device;

depositing a gate material over the gate dielectric for the first device;

forming at least one gate electrode from the gate material for the first device; and

repeating, for the second device, the forming a plurality of channels, depositing connector material, forming a gate mask, removing the connector material, depositing channel material, forming a gate dielectric, depositing a gate material, and forming at least one gate electrode.

19. The method of claim 18 wherein a depth of each of the plurality of channels ranges from about 1000 Å to about 2000 Å into an upper surface of the first layer.

20. The method of claim 18 wherein a width of each of the plurality of channels ranges from about 1500 Å to about 2500 Å.